Project Name	Small pyramids for Light trapping in silicon solar cells
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Project Summary	A solar cell is a device that changes sun light into electricity. For a solar cell to be effective and efficient, it is necessary that most of the sun light be absorbed in the device without reflection. As polished silicon has 40% reflection, surface texturing reduces the reflection down to 10% as well as enhances the path length of light so that the probability of absorption of photons in silicon increases. Current commercial silicon solar cells have upright pyramids of size 5-10 μm on the front surface to reduce reflection of light. But the silicon surface with smaller (~1 μm) sized pyramids has the same reflectance (~10%) as larger pyramid sized surfaces. With the same reflectance as larger sized pyramid surfaces, smaller pyramid surfaces have not only the potential of having higher open circuit voltage due to better surface passivation but are also required for silicon based tandem devices where the top layer has to be deposited by spin coating. Together with the above mentioned benefits, the smaller sized pyramids on the surfaces are also beneficial for certain contact printing technologies such as aerosol printing and ink jet printing. The small pyramid fabrication project is an attempt to create small, uniform sized pyramids on the crystalline silicon wafer surface. Surface texturing with anisotropic etching in potassium hydroxide (KOH) will be used for this project. The size and uniformity of these pyramids can be tuned with texturing chemistry and texturing time. For example higher concentration of surfactant (150 ml GP Solar Alkatex zero) and a shorter time etching (5 minutes) results in a pyramid size of about 600-1000 nm. All processing conditions will require thorough characterization to produce relevant statistics for size and uniformity control. In this project, we will study the effect of surface texturing chemistry and texturing time on the size of pyramids on n-type wafers and design the experimental processes to achieve smaller sized pyramids. We will be using scanning electron microscope (SEM) to investigate the size and uniformity of the pyramids. If time permits, we will compare the 3D images obtained from SEM with the images obtained from AFM. We will study the potential improvements in the solar cells efficiency by studying the surface passivation of these wafers by analyzing the minority carrier lifetime after deposition of surface passivation layers such as amorphous silicon. For this study we will use n-type wafers.
REU Work Plan	1. Students will familiarize themselves with the silicon surface texturing process and related chemistry 2. Students will design and run the experiments based on the information in the literature provided and the guidance of the mentor. 3. They will work with the mentors and other students in the lab to characterize the pyramid shape and size with Scanning Electron Microscope (SEM). For this students will go through the SEM training. 4. The students will design and implement the process flows to control pyramid size with KOH texturing and characterize the structures.